AN UNITY BIT CODER WITH SUPERIOR OVERLOAD PERFORMANCE

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By

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CERTIFICATE

This is to certify that the thesis entitled "A UNITY BIT CODER WITH SUPERIOR OVER LOAD PERFORMANCE" by Aditya Kumar Verma has been carried out under my supervision and has not been submitted elsewhere for a degree.

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ABSTRACT

In a linear delta modulator (LDM) system relatively small value of step size gives rise to slope overload noise, while large value of step size increases granular noise. This present thesis reports various methods of modifying the LDM system for improvement of its overload performance. Some of them are developed in the laboratory which finally gave rise to better overload performance than the LDM. Results of the developed systems have been included.

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CHAPTER 1

INTRODUCTION

1.1 Linear Delta Modulator:

A linear delta modulator (LDM) produces binary pulses at its output which represent the sign of the difference between the input and feed back signal - hence the prefix 'delta', Fig.1.1.0(a) The modulation process is linear as the local decoder, i.e. an integrater, is a linear network. Delta modulator acts as an analogue to digital converter having an analogue input signal x(t) and a binary output signal L(t). The rate of occurence of each binary pulse is directly proportional to the instantaneous slope $\dot{x}(t)$. If the slope of the input signal x(t) is positive then output waveform L(t) has more positive values than negative ones. The situation is reversed when x(t) has a negative slope. The step size is assumed to be a constant in linear Delta Modulation (LDM) i.e. there is no modification done in step size in accordance with the changing slope characteristics of the input signal. The signal fed back from the local decoder to differencial amplifier is simply the sum of all previous transmitted samples.

1.2 Types of Error in DM:

There are two types of errors found in the delta modulation systems:

i) Slope overload noise
ii) Granular noise

i) Slope overload noise: If K is a step size and τ is the sampling period in seconds, K/τ will be the highest input rate of change which D.M. codec can follow and it is called the maximum slope tracking capability of the D.M. system. Whenever slope of the input signal exceeds $K.f_s$, where f_s is the sampling frequency, the coder is unable to track the input signal and this gives rise to what is referred to as the slope overload noise, as shown in Fig. 1.1.0.

ii) Granular noise: It refers to the situation when the slope of the input signal is such that the coder is able to track the input, and the granular noise is the difference between the approximated and the actual signals, as shown in Fig. 1.1.1

The slope overload noise is dominant of the two types of noise when the step size is too small, whereas the granular noise is more when the step size is too large. In order to reduce the total noise power one must optimize the step size for both the regions of the slope of the signal.

1.3 Adaptive Delta Modulation:

It is apparent that a fixed step size will not give an optimum performance in terms of the minimum output noise power. But, if the step size is varied in accordance with

the instantaneous slope of the input signal, i.e., increase the step size under slope overload situation and decrease it when the slope becomes smaller than the nominal slope tracking capability of the coder, the performance will improve significantly. This is achieved with the help of adaptive delta modulators (ADM). An ADM is a modification of LDM in which the step size changes according to the slope of the signal. The adaptation scheme in an ADM can be either of syllabic or instantaneous type. Syllabic companding systems are characterised by 'continuous' adaptation of the step magnitude and have been developed for reproducing telephone quality speech at operating frequencies of the order of 40 KHz, while the instantaneous compandors usually incorporate a discrete adaptation algorithm in the sense that the step size is changed at every sampling instant by a specific factor, - more precisely, by one of two specific factors. Here the encoder responds to the instantaneous variation in the analogue signal and is suitable for encoding both speech and television signals.

The most interesting syllabic systems are "Digitally Controlled Delta Modulation (DCDM)" by Greefkes [1], "Continuous Delta Modulation" by Greefkes and de Jager [2] and "Dual Mode Coder-Decoder" by H.R. Schindler [3].

In DCDM, a uniform coder (UC) is used at the transmitter and a uniform decoder (UD) at the receiver. The step size K is varied by the output voltages from the modulation level analyser (MLA), (Fig. 1.2), which are controlled by the digital signal y. The magnitude of K is now a function of y and hence of the input signal.

The promising systems under instantaneously adaptive delta modulation are "Adaptive Delta Modulator with one bit memory" by N.S. Jayant [4], "Linear and Adaptive Delta Modulation" by J.E. Abate [5] etc. In Jayant's ADM, the step size is adapted (for a stair-case approximation to the signal input) at every sampling instant, on the basis of comparison between the two latest bits (the present and the last previous). If the two compared bits are similar, the step size is increased. On the other hand, if they are different the step size is reduced.

In case of second order constant factor DM the present bit is compared with the previous two bits. The block diagram is same as shown in Fig. 2.1, except that Z_r is formed with the aid of a two bit shift register and some combinational logic according to the equation:

$Z_r = A_r \text{ Sgn. } (L_r)$, where A_r is an adaptation constant and L_r is a bit at rth sampling interval.

High information delta modulation (HIDM) was conceived by Winkler [6,7] for encoding video signals. HIDM system overcomes tracking deficiency. The step size in this system increases in binary fashion i.e. 2,4,8,16 etc.

The step and pulse responses of these systems are shown in Fig. 1.3.0.

1.4 Step Response of Various Systems:

Fig. 1.3.0 shows the behaviour of the fedback signal [y(t)] for first order (i.e., Jayant's scheme) and second order (where three bits are compared) [10] instantaneous ADM systems when a step input of 0.5 to 39.5 units is applied. The y(t) signal in the second order instantaneous ADM encoder over-takes the step input before the first order one does. The response of the first order system for adaptation constants A = 1.5, B = $\frac{1}{1.5}$ - the hunting oscillations do not decay. But damping can be achieved with this system if

$$AB < 1 : A > 1, \quad B < 1$$

However, if AB is considerably reduced, below unity, the SNR is degraded when tracking speech signals. Consequently there is a conflict in selecting this product. But this conflict does not exist with second order system. However, the values of A and B are taken as 1.1 and 0.9. The system response is critically damped but settles faster to the steady state. See Fig. 1.3.0(c).

The response of linear d.m. and h.i.d.m. [10] systems for the same step input as in Fig. 1.3.0 are given in Fig. 1.3.0 (d) and (e) respectively. The linear d.m. and h.i.d.m. codecs have an over-damped and under-damped response, respectively. The second order c.f.d.m. has a response which increases quickly, similar to h.i.d.m. However, it does not have the large over shoot of h.i.d.m. system but it does take few more clock periods to reach steady state.

1.5 Pulse Response of Various Systems:

Here the minimum step size in the waveforms for each encoder is 0.03 units. The second order system has best response to this particular input pulse. The response of linear d.m. codec resembles the pulse response of an R.C. integrator. y(t) waveform of the first order system is unable to reach the peak amplitude of the pulse before this input signal returns to zero volts, whence it exhibits a large hunting oscillation. In second order system the value of its largest adaptation constant $A_4 = 2$, then when overload occurs it responds by doubling the size of the steps in feedback signal at subsequent sampling intervals. HIDM system also behaves in this manner when overloaded.

1.6 Modified DM Systems:

As can ben seen, in these systems more emphasis has

been given to slope overload noise reduction. It was pointed out earlier that the maximum slope tracking capability of the DM coder is Kf_s. This capability should be increased to reduce the slope overload noise, but, at the same time the step size should be kept small to keep the granular noise at an acceptable level. An obvious way to do this is to increase the sampling frequency keeping the step size constant. But, this will increase the transmission bit rate. The previously mentioned ADM systems use variable step size to achieve an adaptive slope capability. But, the increased step sizes reduces the full-load SNR values to some extent. Although called "instantaneous", none of the ADM's described earlier respond instantaneously to say a step change in the input signal level. A faster adaptation scheme has been suggested by Vijoy Kumar[9] where in the step response and the overload SNR is better than other schemes. Of the various modified delta modulation systems suggested by him, the following seem to be more promising in respect of their output signal-to-noise ratio variation with input power. Whenever the error signal exceeds a predetermined threshold, slope overload is declared. The step size under this condition is made two, three or four times the nominal value. In this way the adaptation to a step change in input is made much faster

than in other ADM's. This method has also been generalized to the case of more than one threshold . In this case, the step height is made proportional to the threshold crossed by the error signal. Each of these systems give an SNR greater than 8.9 dB (at full load uniform spectrum input) for a dynamic range of 40 dB input power variation [9]. All these systems use Jayant's algorithm for under-load region of the input, but, vary in the nature of operation in the overload region.

The following table shows the dynamic input power range and the peak SNR for the different systems. It can be seen from the table that the systems have more or less similar results.

Systems	Overload dynamic range (dB)	Peak SNR (dB)	Peak SNR Occuring at input power level (dB)
1. LDM	10.0	13.0	4.0
2. Threshold detection taking 3 times step	42.0	19.2	15.0
3. Threshold detection taking four times step	43.5	20.0	18.5
4. Detection with different thresholds	43.75	22.0	16.0

1.7 Transmission of Overload Information:

Vijoy Kumar has further suggested some methods of transmitting information regarding occurence of the overload to the distant receiver, which is the main problem associated with threshold detection.

i) Whenever slope overload occurs we code the slope magnitudes such that the bit stream itself carries this information.

ii) Whenever overload occurs, shift the transmitted pulse in time suitably. At the receiver, if a pulse does not occur at the normal time instant but at some displaced time, we take the displaced bits as code bits corresponding to the overload slope levels. The difficulty in this method is to detect the shifted pulses unambiguously at the receiver particularly when the channel is noisy.

iii) The third method might be to increase the width of the transmitted code pulses corresponding to the slope overload situation. At the receiver, if a pulse of longer duration occurs, it should be taken as a code bit.

The second and third methods have the constraint that one cannot use 100 percent duty cycle pulses for transmission. This will decrease the transmitted signal

power and thereby, the signal may become more vulnerable to the effects of the channel noise.

iv) Another possibility is to use one extra channel for the transmission of overload information. One arrangement in this can be shown in Fig. 1.4.0. Whenever pulses occur simultaneously at a sampling instant on both the channels, they will be treated as constituting the code for the overload slope magnitude. By this method, we can detect four slope levels. The advantage of this method is that one does not need extra time for transmission of the overload information. The main drawback of this method is the resultant reduction in the capacity of the system.

Out of the modified systems where fixed step of greater amplitude is taken whenever overload occurs, the peak SNR of "Detection with different thresholds" is 2 dB better than that where a 4 times constant step is taken, but at the cost of increased hardware complexity and transmission problem. Hence we choose "Threshold detection taking 4 times step" as the system having the best performance amongst all the methods suggested. From Fig. 1.5.0 it is clear that SNR characteristics of modified system is superior to Jayant's in the slope overload region.

1.8 Scope of Work:

In adaptive delta modulator schemes we have observed that "Jayant's method of ADM with One Bit Memory" where variable step sizes are used to achieve adaptive slope capability is an attractive method. An ADM coder with one bit memory has been hardware realized. The details of the hardware realization have been given in Chapter 2. But this method takes time to build up the step amplitude and thus fails to track the signal quickly. On the other hand, in the modified systems whenever overload occurs, we switch over to the higher step size instantaneously and thus track the signal in a shorter time. Thus it gives better SNR as compared to Jayant's system in the overload region. Three modified systems, named as MDM type I,II and III are discussed in detail in Chpater 3. Some results of these systems along with that of the LDM have been given in Chapter 4, where their superiority over LDM have been shown. **In Chapter 5 the thesis has been concluded.**

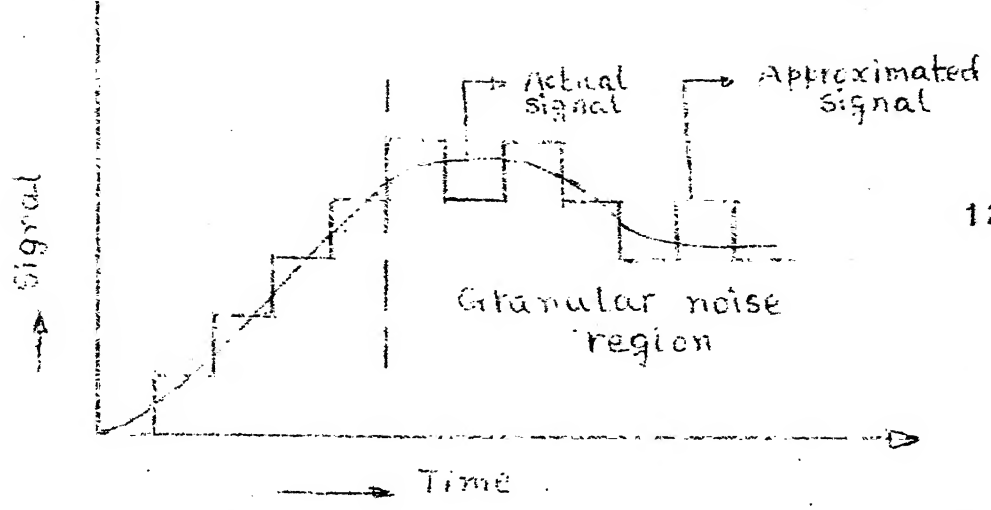


Fig. 1.11 ILLUSTRATION OF GRANULAR NOICE REGION

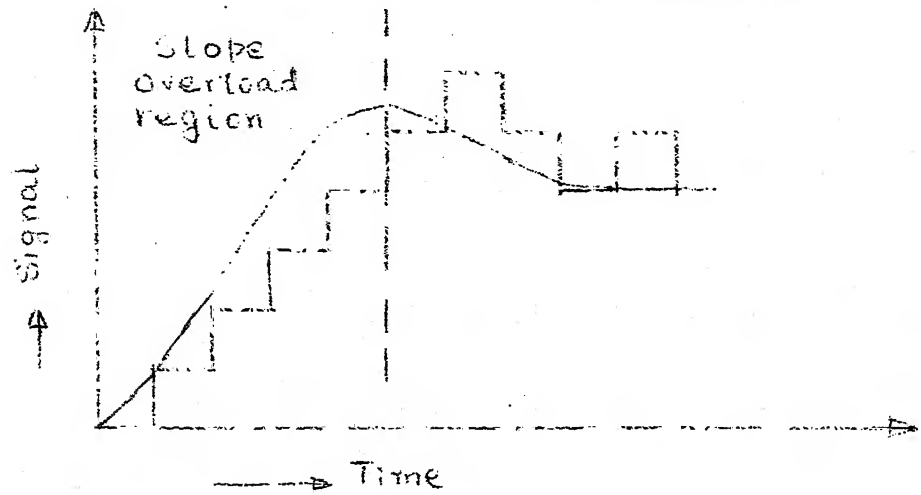


Fig. 1.10 ILLUSTRATION OF OVERLOAD NOISE REGION

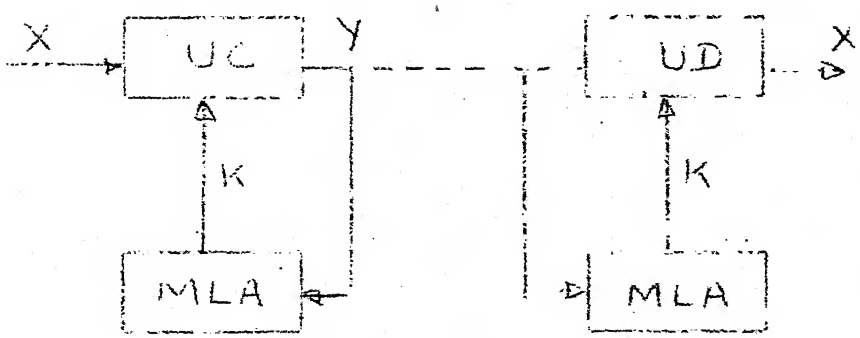


Fig. 1.2.0 BLOCK DIAGRAM OF DIGITALLY CONTROLLED DELTA MODULATOR

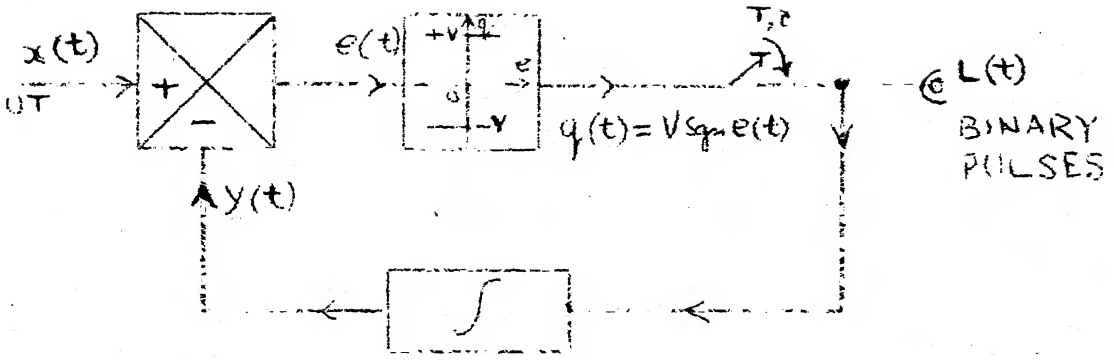


Fig. 1·1·0 (a) LINEAR DELTA MODULATOR SYSTEM.

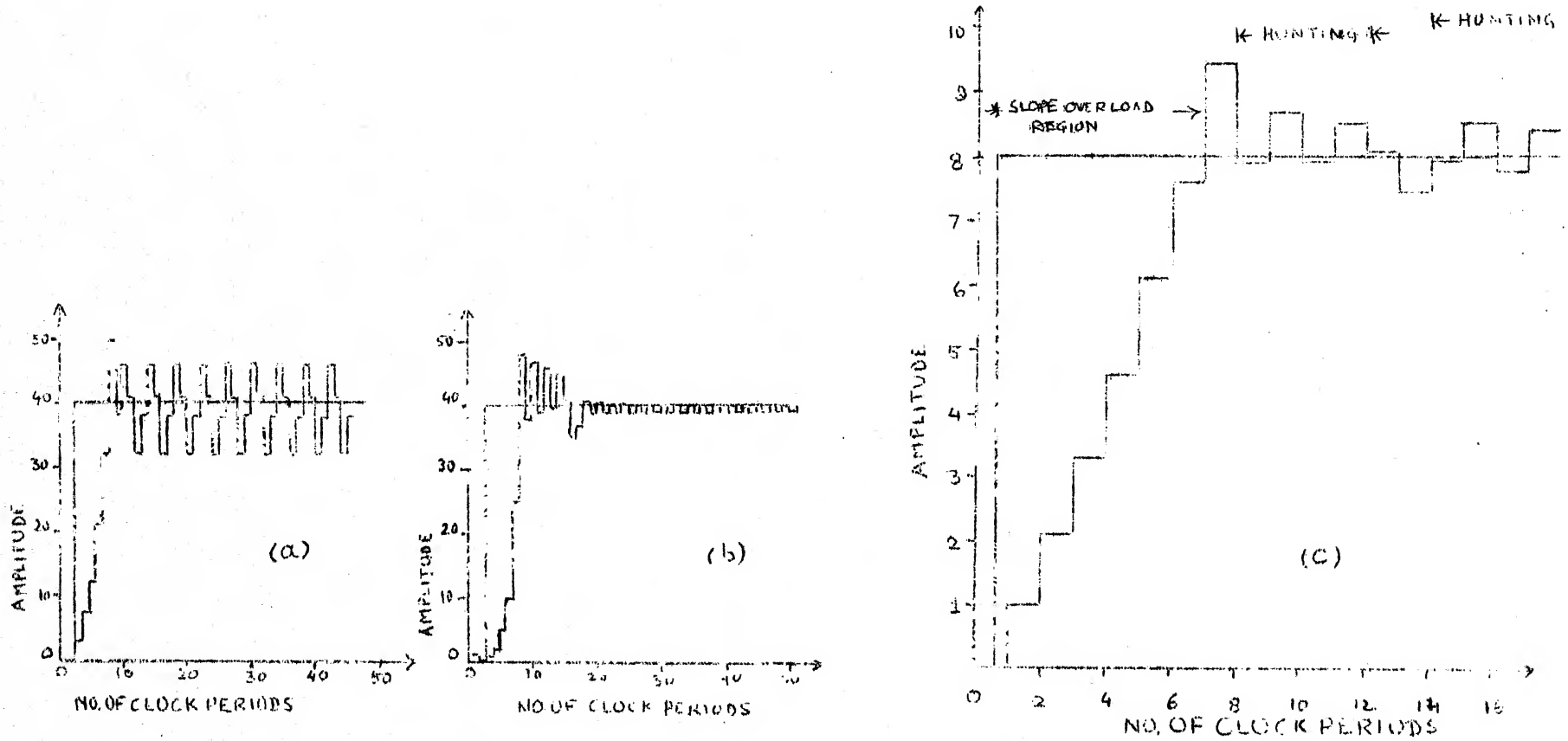
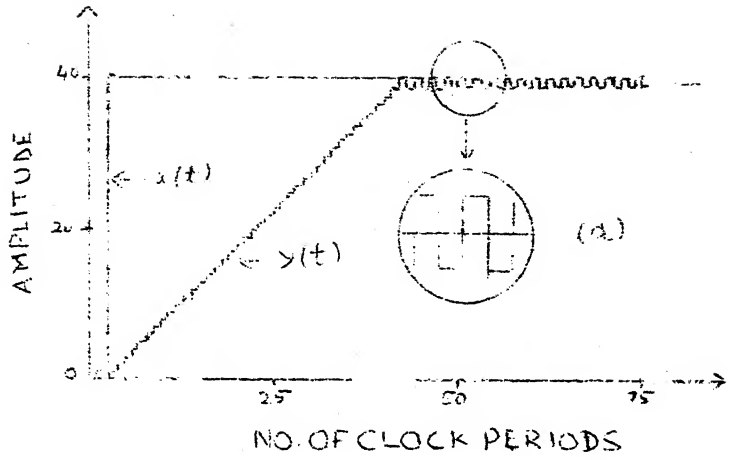


FIG. 1·3·0 STEP INPUT RESPONSE OF C.F.D.M. CODECS: (a) 1ST ORDER; (b) 2ND ORDER; (c) ADM WITH ONE BIT MEMORY. THE INITIAL STEP SIZE OF y(1) IS UNITY. ADAPTATION CONSTANTS IN (c) ARE (A=1·5, B=0·5), (C)→(A=1·1, B=0·9)



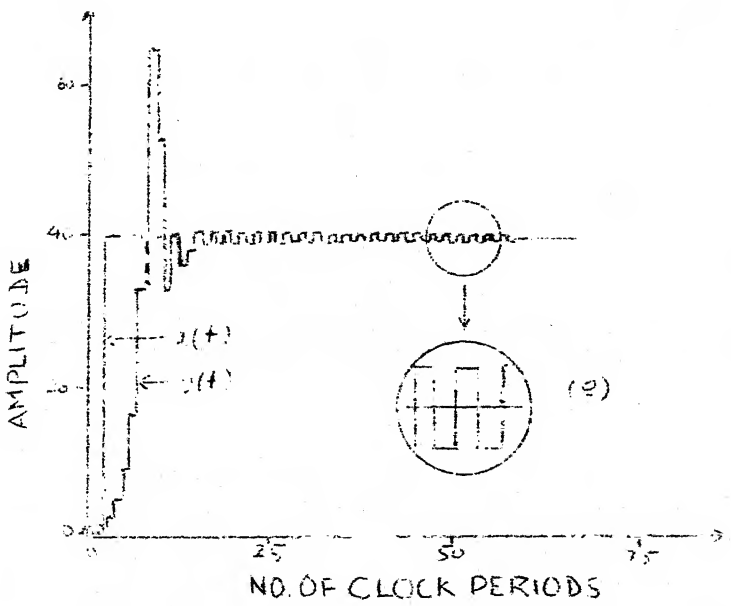
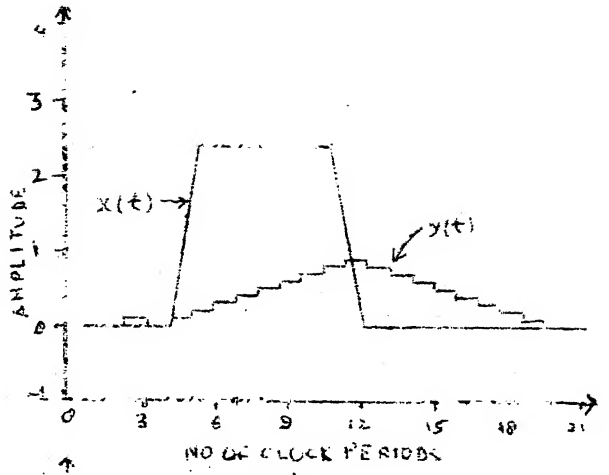
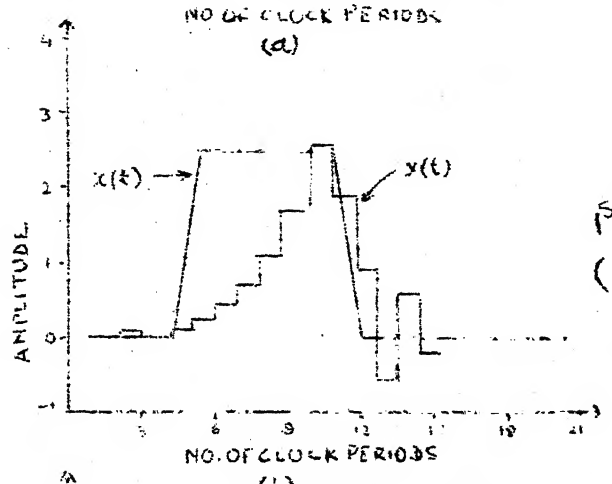


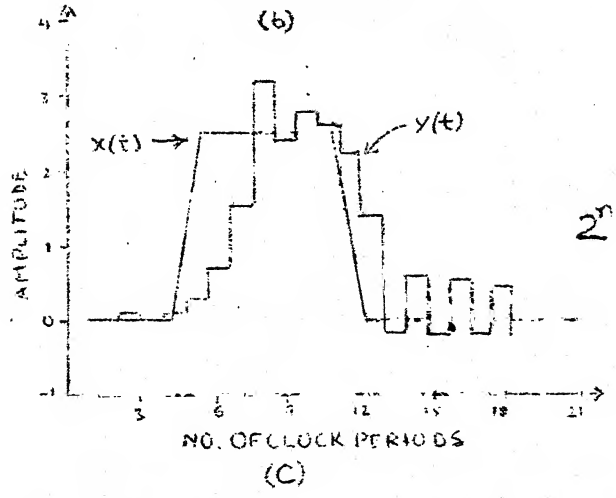
FIG. 1.3.C. STEP RESPONSE OF (d) LINEAR DM; (e) H.I.D.M.



LINEAR DM



1st ORDER SYSTEM
(JAYANT)



2nd ORDER SYSTEM

FIG. 1.3.1 PULSE RESPONSE OF VARIOUS SYSTEMS

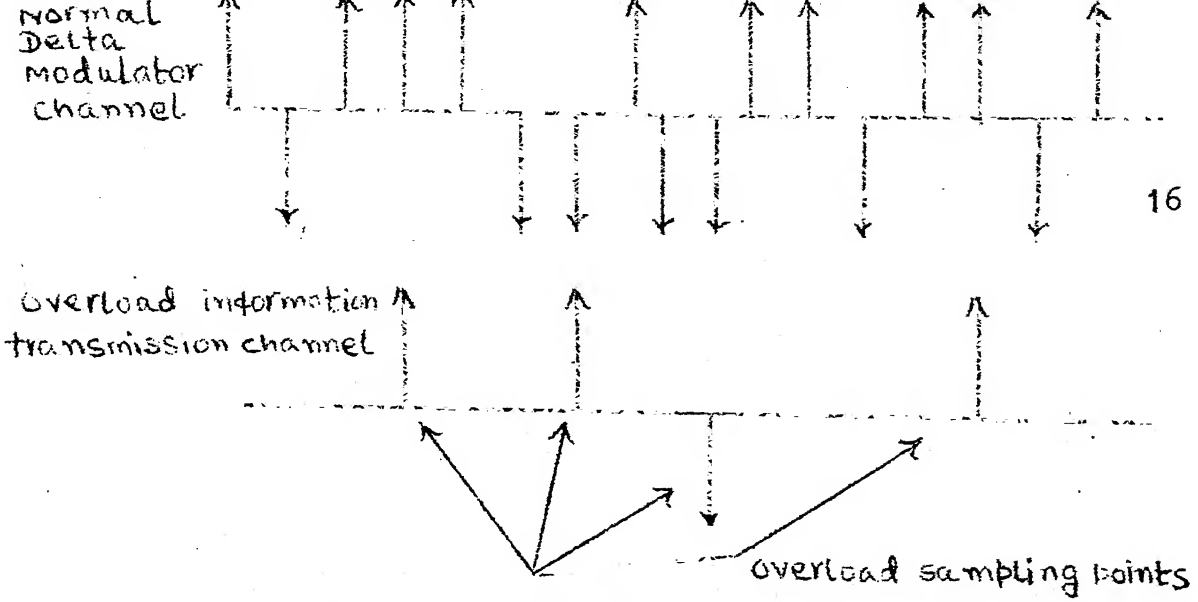


Fig. 1.4.0. TRANSMISSION OF OVERLOAD INFORMATION WITH EXTRA CHANNEL

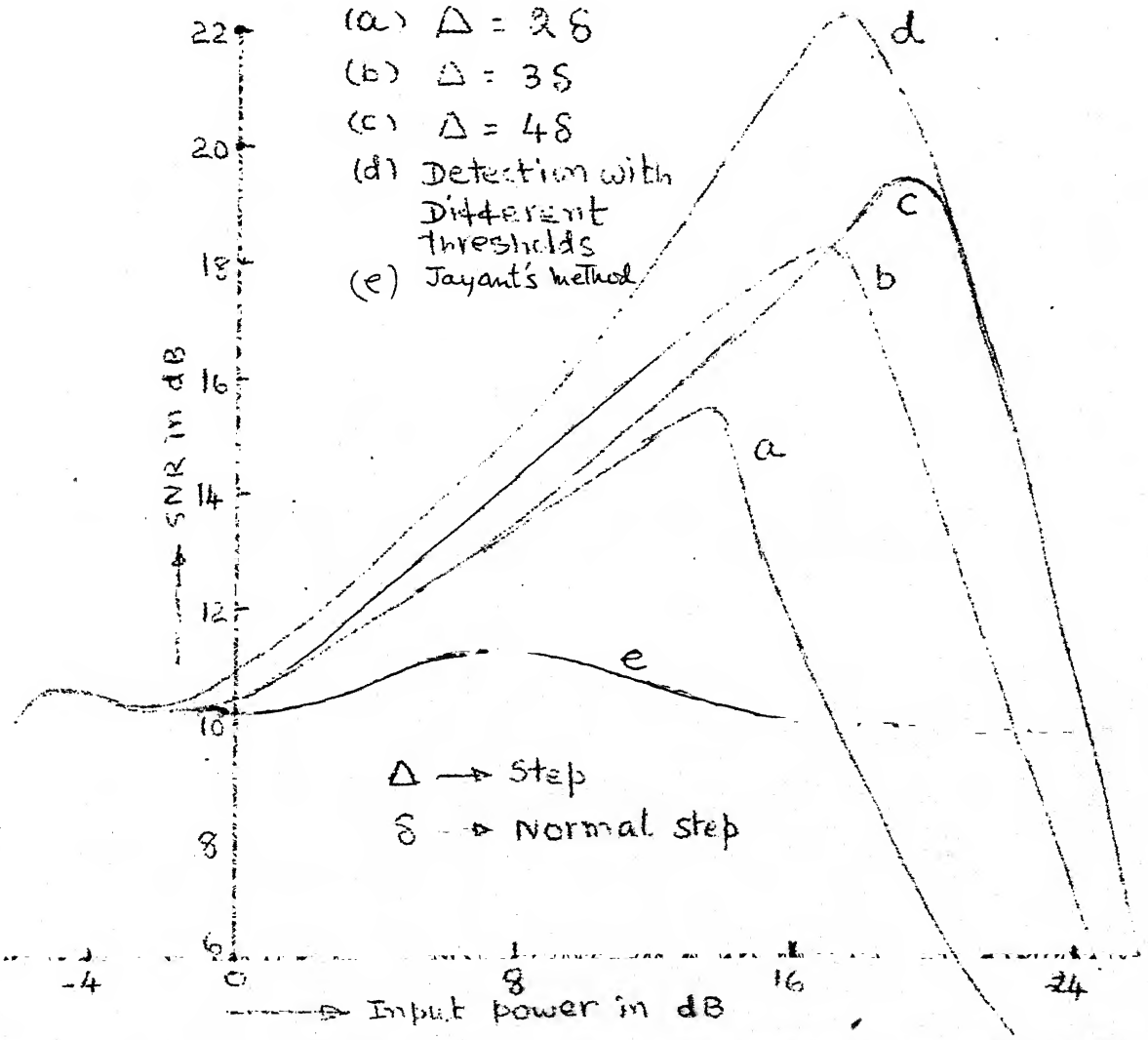


Fig. 1.5.0 PERFORMANCE OF MODIFIED DM SYSTEMS

CHAPTER 2

ADAPTIVE DELTA MODULATOR

Of the different instantaneous ADM's described in Sec. 1.3, Jayant's scheme has found wide acceptability. This is because of the simplicity of the adaptation logic in this scheme. The hardware implementation of this ADM is also less involved than the other methods described. In Sec. 2.1 we have described Jayant's ADM with one bit memory in detail, and in Sec. 2.2, a hardware description of this coder developed in the laboratory has been given.

2.1 ADM with One Bit Memory:

The encoder of the ADM with one bit memory is shown in Fig. 2.1.0. The output binary waveform L(t) is of course transmitted after — suitable processing (e.g., filtering, modulation etc.) to the receiver. It is also connected to the adaptation logic in the feedback network. This logic has a one bit digital delay D_b so that it can inspect the binary level of the L(t) signal at the rth sampling and also at the previous (r-1)th sampling instant. Let the corresponding values of L(t) be L_r and L_{r-1}, respectively.

If L_r and L_{r-1} are both ones or zeros it indicates that the error has not changed sign for two successive

clock periods which means that the coder is not able to track the input signal properly. Therefore, some increase in the size of the step fed back to the difference circuit is needed. On the other hand, if L_r and L_{r-1} are different the error has changed polarity between successive clock periods. This suggests that the step height in y(t) should be reduced in magnitude.

The exclusive-OR — gate in Fig. 2.1.0 has a logic one output when L_r and L_{r-1} are different and a logic — zero when they are either both ones or both zeros. Suppose at a sampling instant the output of the Ex-OR is a logic 'one' and switch is moved to the negative voltage source. If the output from the Exclusive-OR is a logic zero the switch connects the +ve voltage to the input of the multiplier. This input Z(t) consists of impulses of strength -B or +A depending on whether the switch is connected to the negative or positive voltage source.

At a particular sampling instant r, $Z(t) = Z_r$ where

$$Z_r \begin{cases} = \text{impulse A, if } L_r = L_{r-1} \\ = \text{impulse B, if } L_r \neq L_{r-1} \end{cases}$$

The final waveform y(t) fedback to the error point is the integral of m(t) where m(t) is the waveform at the output of the multiplier. At the rth sampling instant m(t) is m_r

and is formed by multiplying the previous value of m_r by Z_r

$$m_r = Z_r \cdot m_{r-1} \qquad (2.1)$$

The production of m_{r-1} requires the use of an analogue delay (A.D.) of one bit duration. As m_{r-1} can occupy a wide range of values, there are practical difficulties in producing an analogue delay having a wide voltage dynamic range.

Z_r is an impulse and consequently m_r is also an impulse with the result that the waveform y(t) contains steps of varying height. If y_r is the value of y(t) at the rth sampling instant, then

$$y_r = y_{r-1} + m_r \qquad (2.2)$$

This is because m_r is integrated to give the new value of y(t), namely y_r. The integral of an impulse of strength m_r is a step of height m_r.

Substituting for m_r from Eqn. (2.1) in equation (2.2) gives

$$\Delta y_r = y_r - y_{r-1} = Z_r - m_{r-1} \qquad (2.3)$$

As Z_r is either A or -B, the ratio between two successive steps in the feedback waveform differ by a constant factor Z_r. and because of this important property

that this type of encoder has also been called a constant factor delta modulator (CFDM). This name distinguishes it from other delta modulator encoders which have short memories in the feed-back loop and are of the instantaneous adaptive type.

2.1.1 Overload Condition: The impulse m(t) applied to the integrator change strength by a constant factor of either A or -B at every clock instant, hence the adaptation is instantaneous. This is illustrated by considering the situation when the encoder is suddenly overloaded by a positive step input results in L(t) having a sequence of all 'ones', i.e. $L_r = L_{r-1}$, over a no. of clock periods. When overload occurs the impulse at the output of the multiplier has a value of one unit. Because of logical output waveform is a sequence of all 'ones', a corresponding sequence of A adaptations occur and the impulse sequence applied to the integrator increases as A, A^2, A^3,...,A^n units. The feedback voltage at the output of the integrator sums the impulses applied to its input such that after n-A-type adaptations, the feedback voltage has increased to

$$y_r = \sum_{r=0}^{n} A^r \qquad (2.4)$$

If the overload condition is caused by a negative step, the output binary sequences is all 'zeros', but as L_r still equals L_{r-1} in this sequence, the adaptation remains

to A-type and y_n is

$$y_n = - \sum_{r=0}^{n} A^r$$

assuming that the initial impulse to the integrator is -1 unit.

2.1.2 Adaptation Constants: In order for the sequence of A adaptations to result in the increase of the feedback signal y(t) the value of A must be greater than unity. In this way the impulses A^r applied to the integrator increase their strength with the increasing no. r of clock periods. When y(t) exceeds the level of the input signal x(t) there will be a change in the sign of the error signal, $L_r \neq L_{r-1}$, and a B adaptation will be produced. The encoder is now required to generate a smaller impulse at the input to the integrator in order to reduce the magnitude of the error signal at the next clock instant. This reduction is achieved by making $B < 1$. It is seen that for a band-limited random input signal the optimum product AB will be close to unity. If $A = B = 1$, the encoder is just a linear delta modulator. The values of A and B are chosen same as Jayant [8] suggested i.e. $A = +1.1$ and $B = -0.909$.

2.1.3 Step input response: If we consider the step input application to first order c.f.d.m. encoder having an

amplitude of 8 units. If we take initial step in the y(t) waveform as one unit, then the behaviour of the various signals in the encoder at the successive sampling instants r = 0,1,2... is shown in Table 2.1. The values of y_r and m_r are given by equations

$$y_r = y_{r-1} + m_r \qquad (2.1)$$

$$m_r = Z_r \cdot m_{r-1} \qquad (2.2)$$

The value of y_r is calculated for the adaptation constants, namely A = 1.1 and B = -0.9. The response y(t) is shown in Fig. 1.3.0(c) — where it can be seen that y(t) hunts about the step input x(t) with a 10101100... pattern. If adaptation constants are related as $A = \frac{1}{B}$, then no decay occurs. Slope overload noise and hunting situations are also indicated in Fig. 1.3.0(c) The response of the system shows slow decay.

2.2 Experimental Development of ADM:

An adaptive delta modulator has been fabricated using Jayant's adaptation logic. The detailed block schematic of this coder is shown in Fig. 2.2.0.

A difference amplifier is used in order to get the error between the bandlimited signal input x_r and y_r from the local decoder feedback network. The error voltage e_r is fed to comparator keeping other terminal grounded. The

Table 2.1

r	L_r	L_{r-1}	Z_r	$m_r = Z_r \times m_{r-1}$	$y_r = m_r + y_{r-1}$	y_r $\Lambda=1.1$ $B=0.9$
0	1	.	.	1	1	1.0
1	1	1	Λ	$\Lambda \times 1 = \Lambda$	$1+\Lambda$	2.1
2	1	1	Λ	$\Lambda \times \Lambda = \Lambda^2$	$1+\Lambda+\Lambda^2$	3.31
3	1	1	Λ	$\Lambda \times \Lambda^2 = \Lambda^3$	$1+\Lambda+\Lambda^2+\Lambda^3$	4.64
4	1	1	Λ	$\Lambda \times \Lambda^3 = \Lambda^4$	$1+\Lambda+\Lambda^2+\Lambda^3+\Lambda^4$	6.10
5	1	1	Λ	$\Lambda \times \Lambda^4 = \Lambda^5$	$\sum_{n=0}^{5} \Lambda^n$	7.71
6	1	1	Λ	$\Lambda \times \Lambda^5 = \Lambda^6$	$\sum_{n=0}^{6} \Lambda^n$	9.48
7	0	1	$-B$	$(-B) \times \Lambda^6 = -B\Lambda^6$	$\sum_{n=0}^{6} \Lambda^n - B\Lambda^6$	7.88
8	1	0	$-B$	$(-B)(-B\Lambda^6) = B^2\Lambda^6$	$\sum_{n=0}^{n=6} \Lambda^n - B\Lambda^6(1-B)$	8.66
9	0	1	$-B$	$(-B)(B^2\Lambda^6) = -B^3\Lambda^6$	$\sum_{n=0}^{n=6} \Lambda^n - B\Lambda^6 + B^2\Lambda^6 - B^3\Lambda^6$	7.96
10	1	0	$-B$	$(-B)(-B^2\Lambda^6) = B^4\Lambda^6$	$\sum_{n=0}^{n=6} \Lambda^n - B\Lambda^6 + B^2\Lambda^6 - B^3\Lambda^6 + B^4\Lambda^6$	8.59
11	1	1	Λ	$(B^4\Lambda^6) \times \Lambda = B^4\Lambda^7$	$\sum_{n=0}^{6} \Lambda^n - B\Lambda^6 + B^2\Lambda^6 - B^3\Lambda^6 + B^4\Lambda^6 + B^4\Lambda^7$	8.02
12	0	1	$-B$	$(B^4\Lambda^7)(-B) = -B^5\Lambda^7$	$\sum_{n=0}^{6} \Lambda^n - B\Lambda^6(1-B+B^2-B^3-B^3\Lambda+B^4\Lambda)$	7.40

output of the comparator is thus binary (0,1). When error e_r is positive, output of comparator is 'one' otherwise 'zero.' The output of comparator goes to the D-flipflop in order to synchronize the comparator output with the clock. We obtain one past bit by shifting DFF output to right by one clock pulse period and feed DFF and shift register outputs to the exclusive OR gate. We get 'zero' output when the present and the past bit are both either 'zero' or 'one'. It indicates that error has not changed sign for two successive clock periods and some increase in the size of the step is required for minimizing error voltage. On the other hand if the present and the past bits are different, we get as the output of the Ex-OR gate a 'one', which indicates that the error voltage e_r has changed polarity between two successive clock periods. It suggests that some reduction in step size is necessary.

Thus according to the state of the Ex-OR output linear gates (1) or (2) is switched on to operate either the amplifier of gain 1.1 or the amplifier of gain 0.9 . These d.c. levels are fed to non inverting amplifier to meet the sensitivity requirement of the Sample & Hold which samples the level for 'on' time of the clock pulse and holds the same level for the 'OFF' time of the clock pulse. The analogue

delay of one clock period is achieved through the sample and hold operation. The previous level of the sample and hold is multiplied by the present level. At every clock pulse the new level is sent to integrator and modified y_r comes closer to the original signal.

2.2.1 Circuit Description of Comparator and Quantizer:

Consider the block diagram shown in Fig. 2.2.1. The differential amplifier is designed to amplify the difference between incoming bandlimited signal x_r and feedback signal y_r through local decoder such that error signal e_r always remains greater than five millivolt to get binary output from the comparator 1. This signal is fed to the DFF-1 to get the signal synchronized with the original clock. DFF output and shift register (S-R-1) output which is also synchronized with the clock, are fed to Exclusive-OR-1 gate to get the desired logic as explained earlier in the section 2.1.

2.2.2 Clock Generator:

The details of the clock generator is shown in Fig. 2.2.2. A NE 555 is used as an astable multivibrator constituting the basic pulse generator. The frequency of the multivibrator is adjusted by choosing proper values of R_1, R_2 and C, in the formula given below.

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

The output of the astable multivibrator is fed to a monostable multivibrator (N74123) through the unity gain buffer amplifier. The monostable multivibrator is used to keep the on period of the incoming clock as small as possible. Lowering the 'on period' of the clock reduces the pulse width which ultimately results in better stair-case approximation of the input signal x_r. The negative pulses are obtained by inverting the one shot output. These pulses are fed to the sample and hold circuit as described later.

2.2.3 Adaptation logic:

The detailed circuit diagram shown in Fig. 2.2.3 realizes the adaptation logic described earlier. In the — figure the 2N2369 transistor (Q_1) is used for switching the signal coming from the Ex-OR output. When the Ex-OR output is '1' then the 2N2369 transistor (Q_1) is switched on a voltage at A point is less than 0.6V which is unable to switch on the second transistor (Q_3) and it remains in cut off condition. At the point B full voltage remains which switches on the third transistor (Q_4). Final output is 'zero' when input to the first transistor (Q_1) is 'one'. Hence output of the opamp (AV_1) giving gain (K=1.1) remains zero. At the same instant when the Ex-OR output is '1' the input to transistor (Q_2) is '0' and it remains

cut off. Hence the voltage at collector of (Q_2) goes to the opamp (AV_2) giving gain (K=0.9) which is then inverted. Thus we select '-B' when the Ex-OR output is '1'. When the Ex-OR output is '0', transistor (Q_4) is cut off and the voltage n_{r-1} is applied to opamp(AV_1) through the transistor (Q_4) with the gain of 1.1. This level is inverted twice as it goes through two inverting amplifiers hence we get adaptation constant as +A. If clock pulse width τ is very small, these d.c. levels can be treated as d.c. impulses, which are input to sample and hold circuit. These levels charge the 1000 pF capacitor only when the FET switch is closed . The FET switch is closed when the switching transistor 2N2904 is saturated by a — negative going clock pulse. The switching transistor remains in cut off condition during 'OFF' period of the clock. Hence the FET switch is open and capacitor holds that charge until the next clock pulse arrives. Clock pulse 'on period' must be greater than the time constant of the charging network in order to allow capacitor to charge to its maximum value. Any droop in the voltage of capacitor due to bias current of the opamp, external bias is applied through the 'Droop Adjust' network. The output of the sample and hold will be n_{r-1} i.e. n_r will be delayed by one clock period. Now n_{r-1} will be switched to opamp(AV_1) through transistor (Q_2) or (Q_4) depending upon Ex-OR output and it will

be again multiplied by either +A or -B at opamp (AV_1) and opamp(AV_2) respectively. Non-inverting amplifier (AV_3) is used between adaptation logic output and sample and hold input to boost the level so as to get satisfactory performance of the sample and hold circuit. Output of the adaptation logic is fed to the non-inverting amplifier in order to adjust the loop gain for better stability of the system. The output of the amplifier is fed to the integrator whose d.c. gain is about 25 and integration time constant is about 180 μs assuming probability of occurrence of ones or zeros more than five times consecutively. is very low.

The complete circuit diagram of the adaptive delta coder with one bit memory has been shown in Fig. 2.2.4. The output of the integrator, which is a replica of the separate decoder, showed a low frequency jitter. The cause of this jitter was not very clear.

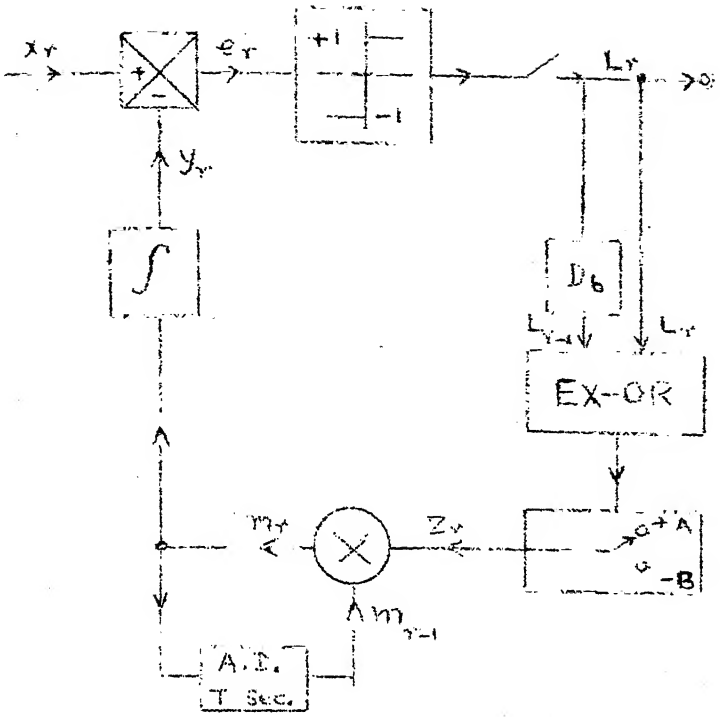


FIG. 2.1.0 FIRST ORDER CONSTANT FACTOR DM ENCODER (AFTER JAYANT)

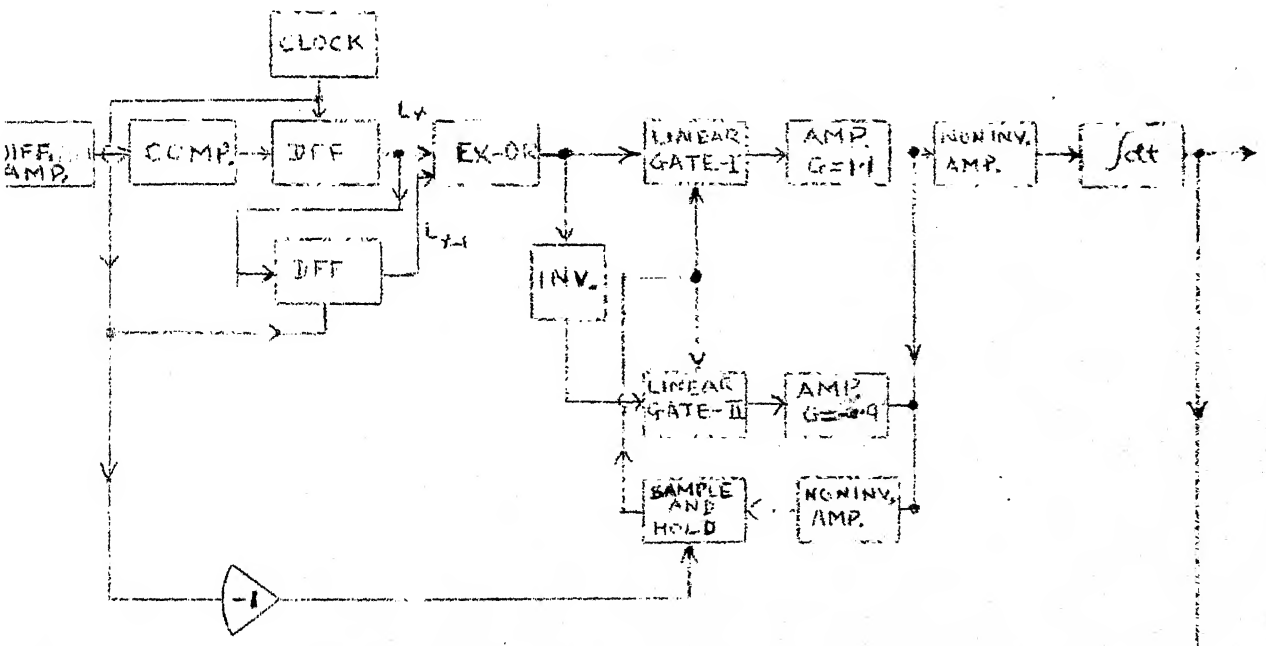


FIG. 2 2.0 BLOCK DIAGRAM OF ADM

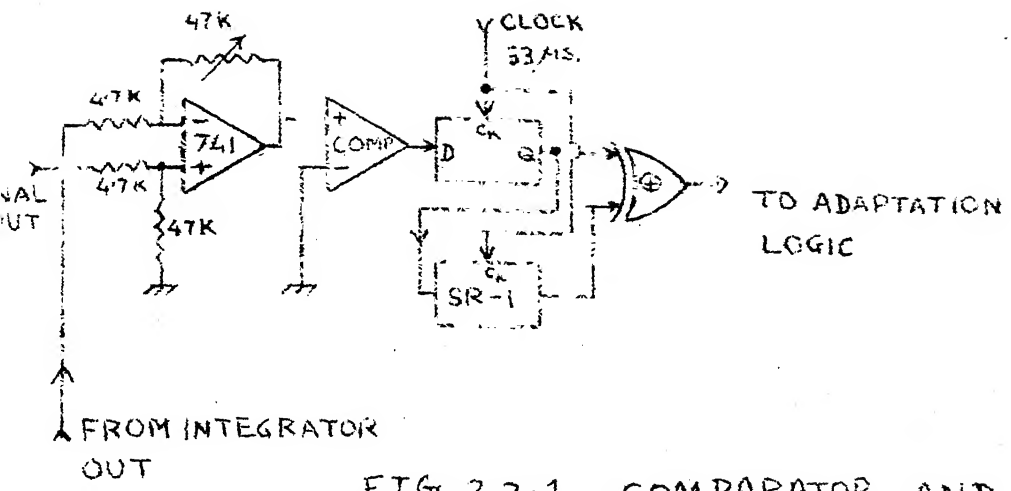


FIG. 2.2.1 COMPARATOR AND QUANTIZER

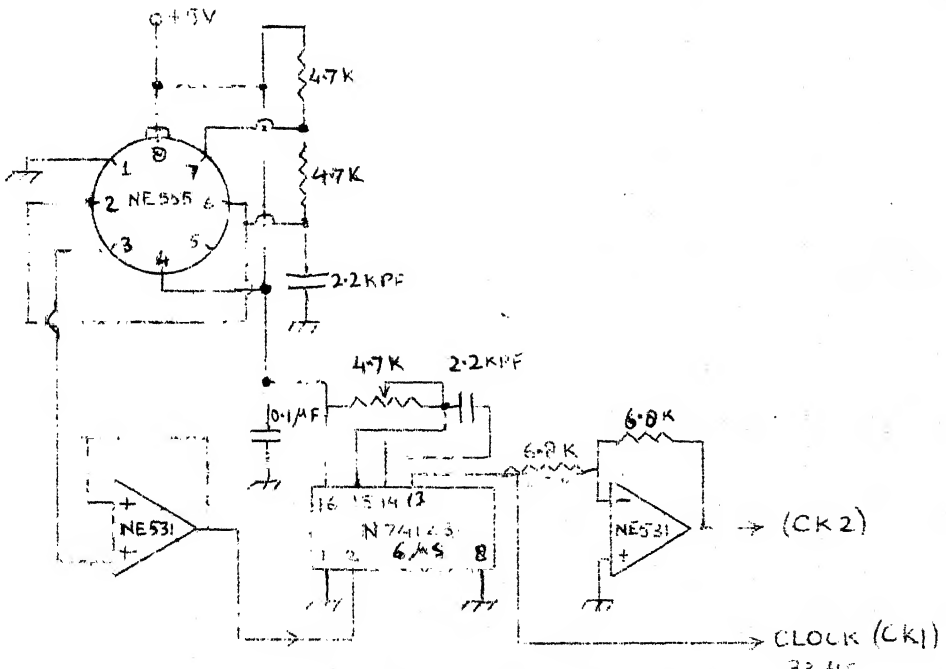


FIG. 2.2.2 CLOCK GENERATOR

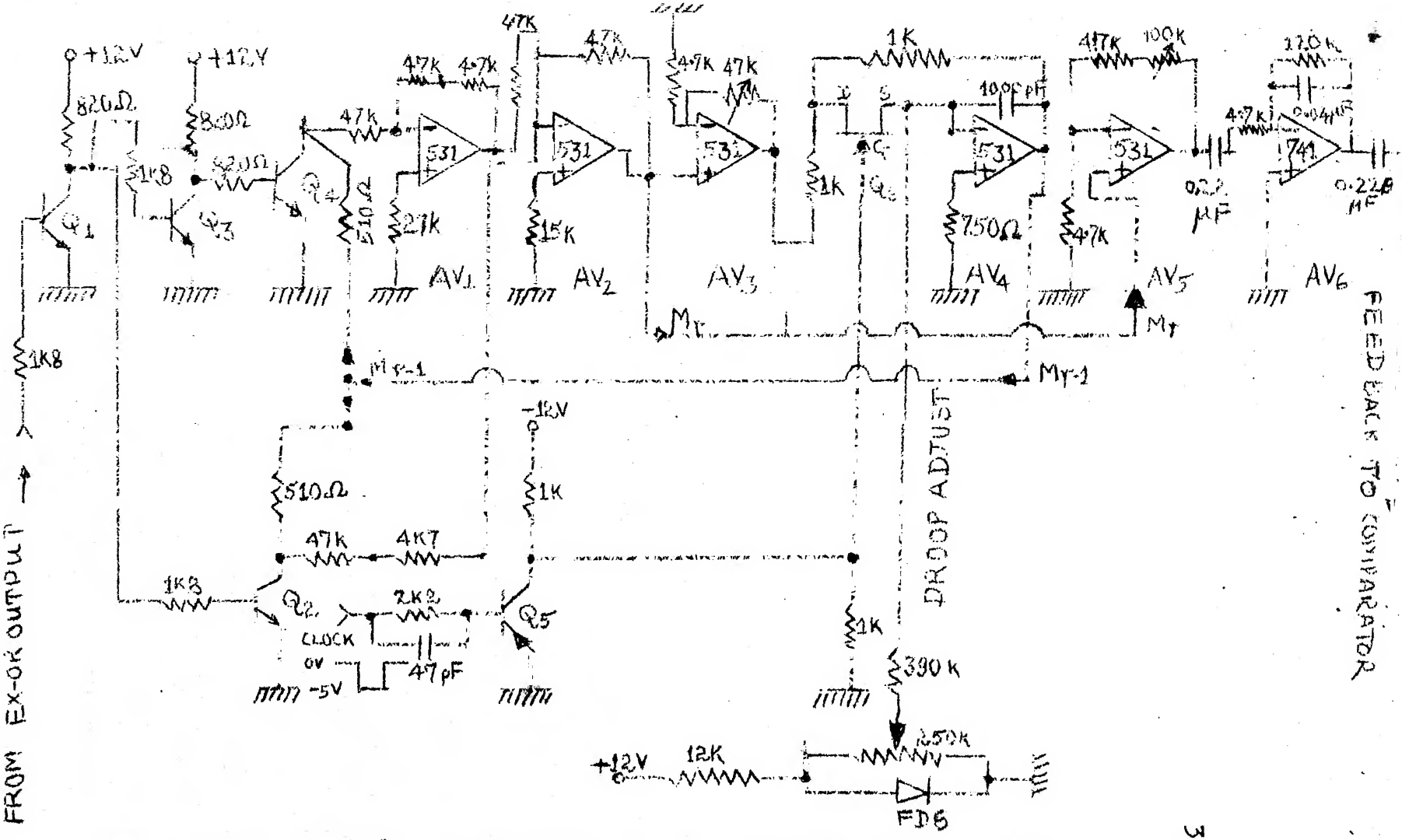


Fig. 2.2.3 : CIRCUIT DIAGRAM OF AN ADAPTATION LOGIC.

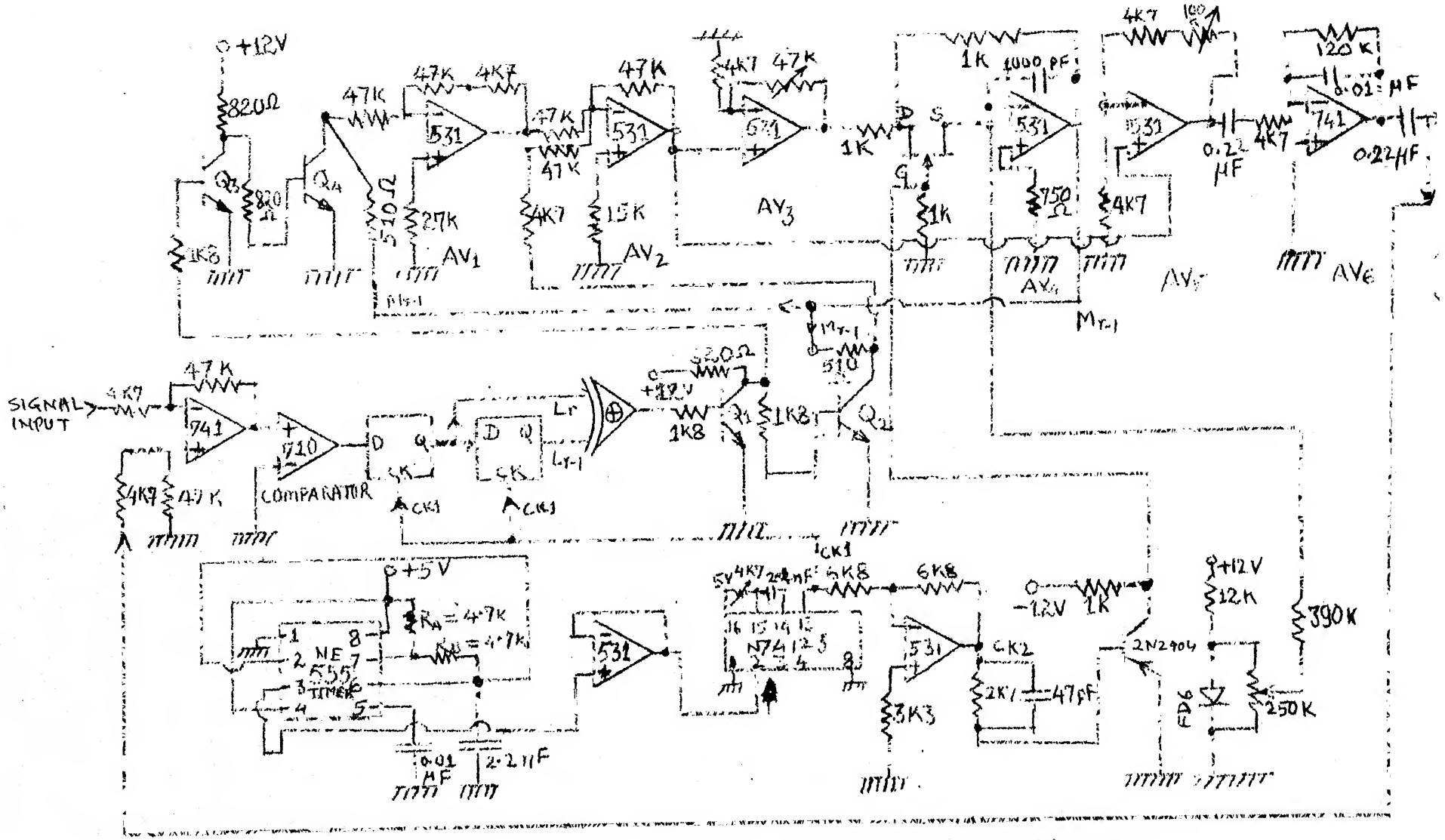


Fig. 2.2.4 : Adaptive Delta Coder With One Bit Memory.

CHAPTER 3

MODIFIED LINEAR DELTA MODULATORS

In this chapter we would describe modifications in LDM for improvement of its performance in the slope overload region. In order to boost SNR in the overload region the step size must be adapted according to the slope of the input signal. Samething can be achieved by increasing the sampling frequency also, but, only at the cost of increased transmission bandwidth. Now when the slope overload occurs, we detect it and modify the step size such that the feedback signal from the local decoder comes closer and closer to the original input signal. Two methods of modifications in the linear delta modulator have been realized experimentally. Performance of those systems have been compared with the performance of the linear delta modulator. Both these methods incorporate a threshold detector in the encoder to determine the occurrence of the slope overload as described in Chapter 1.

3.1 Modified Delta Modulator Type I:

In this method we check the absolute difference of the input and the feed-back signal at each sampling instant. If this absolute difference is greater than some predetermined threshold, we say that overload has occured and we increase

the step size by a specific factor. In this method it is difficult to send information regarding occurance of the overload to the receiver. Fig. 3.1 shows the block schematic of the basic delta modulator alongwith the modifications incorporated for the slope overload detection and thereby increasing the normal step size to some preset value.

In the modified channel we continuously observe the absolute difference between the input and the fedback signal. When it is greater than the preset threshold level, the comparator (CR_2) gives an output of 'one' and this level is utilized in increasing the gain of the amplifier from K=1 (in the case of normal step size) to K= 4 with threshold of 0.8, 1.5, 2.0 volts etc. This modified path is asynchronous as the overload pulses are not synchronized with the system clock. In this case the "overload" pulses may occur more than once in a clock period. This modification, although unusable in a synchronous system, was studied to have an idea about the performance that a wholly synchronous arrangement can approach as a limiting case.

3.2 Circuit Description of the Modified Delta Modulator, Type-I:

The circuit diagram of the modified delta modulator system is shown in the Fig. 3.2. The output of the differential amplifier (DA) is converted to a binary signal

with the help of the comparator (CR_1) keeping inverting terminal at zero potential. Whenever the signal at the positive terminal is high, output of the comparator goes to "one" state otherwise goes to "zero" state. These levels are TTL compatible and fed to the DFF. Now output of the DFF is synchronized with the clock and this level is boosted by the level shifter (Q_1). When DFF output is 'low' it saturates the transistor (Q_1) and the output is 'one' when DFF output is high, it cuts-off the transistor (Q_1) and output is '-1'. These pulses are passed through an opamp (AV_6) of gain (-1) and then through another opamp (AV_7) of gain less than -1 in order to get the phase unchanged. Then these pulses are integrated with the help of the integrator (AV_8). The integrator time constant (about 180 μs) is kept sufficiently high so that feedback capacitor (C_2) should get fully charged with the input pulse as described in the previous chapter.

The output of the difference amplifier is fed to the absolute value detector (AVD) to get an unidirectional error so that the error of both the polarities can be compared at the comparator (CR_2) with preset threshold level. In the AVD when the signal input is greater than zero the output voltage of the AVD will be equal to the input voltage

(e_i). On the other hand, the input voltage is less than zero, the output of the AVD will be ($-e_i$), i.e., if input voltage is e_i and output voltage e_o, we get

$$e_o = |e_i| \qquad (3.1)$$

When the output of the AVD is greater than the preset threshold level, we get "overload" pulses at the comparator output. These pulses are passed through an opamp of gain (-1) in order to make it suitable for switching the PNP driver transistor (Q_3) and then the FET switch (Q_2) when "overload" pulses appear, output of the opamp with gain '-1' gives negative pulse which saturates the transistor (Q_3). Low voltage at the N-channel FET gate switches on the FET and pulses from level shifter through unity gain buffer amplifier are applied to the inverting amplifier (AV_6). Resistor R_{19} is adjusted to get the desired step size increment. These pulses are applied to the integrator (AV_8) through one more inverting amplifier in order to keep the phase unchanged. Results of themodified delta modulator are discussed in next chapter.

3.3 Modified Delta Modulator, Type-II and III:

As mentioned in section 3.1 overload occurs when the absolute difference of the input and feedback signal is greater than the predetermined threshold. It is further stated that the step size is increased to K=4 from the normal step size, K=1, whenever overload occurs irrespective of the clock

rate. But in MDM (Type-II and III) systems, the overload pulses are synchronized with the system clock, hence the step size is increased by the same factor as mentioned above at the occurence of the overload pulses only at the clock instants. Here the advantage is that this modification can be used in a synchronous system while it was not possible in the case of MDM (Type-I).

From the combined block diagram of MDM, Type-I, II and III as shown in Fig. 3.4, it is clear that if the switch S_1 is at position 1 and the switch S_2-S_3 is also at 1, then the circuit determining the sign of the "overload" pulses and suppressing a change of sign within a 3-bit "word" (shown in Fig. 3.3.0 within the dotted box) is now out side the feedback loop of the encoder. But this circuit precedes the line encoder (to be described later) in the transmitter. This kind of delta encoder has been referred to as the MDM (Type-II) system. On the other hand, if the aforementioned circuit is included in the feedback loop of the encoder (as shown in Fig. 3.3.0), it has been referred to as MDM (Type-III).

In the block diagram shown in Fig. 3.3.0, we consider the sequence of overload pulses three at a time. We get

three pulses at the output of one of the S-R flipflops and check the polarity of the first bit pulse. If first pulse is positive then only positive pulses will be passed through data selector from that sequence of three pulses. We allow single polarity pulses in three bit word at a time assuming that the polarity of the 'overload' pulses will not change within the sequence of three pulses. Now when the output of the data selector is high, it increases the normal step size to a preset value and fed to the integrator. The complete logic system can be better understood by different stage waveforms of the system shown in Fig. 3.3.1.

The performance of the modified delta modulator type-I, II and III has been checked separately. Various plots of frequency vs. SNR for all the cases are shown in Chapter 4, and compared with the theoretical simulated results.

3.4 Complete Block Diagram of the Modified Delta Modulators, Type I, II and III:

Fig. 3.4 shows the combined block diagram of the modified delta modulation schemes. (i) When the switch S_1 is at position 1 and S_2-S_3 at position 2, the system is not synchronized with the clock in the feed back loop. This system as such is not usable in practice, but we observed the behaviour and compared it with synchronized systems.

(ii) When the switch S_1 is at position 1 and the switch S_2-S_3 at position 1, the system in loop is called MDM (Type-II) where the local decoder is a simple integrator.

(iii) When the switch S_1 is at position 2 and S_2-S_3 is at position 1, the system in loop is called MDM (Type-III) in which the local decoder is one which does not allow a change of polarity in every three bit word. In this system a distant decoder need not be the replica of the transmitting side decoder. It can be a simple decoder at the receiver side which in turn reduces the complexity of the receiver.

3.5 Line Encoding:

The normal bit stream from an LDM comprises ± 1 type bipolar pulses. The "overload" pulse information will be transmitted by a zero, i.e., not transmitting any level whenever an overload occurs. The sign of the enlarged step will be given by an added bit for every three nominal bits in the transmitted stream. This can be achieved with the help of the scheme shown in Fig. 3.5.0. A +1 added bit will mean a positive step and a -1 added bit a negative step. A zero in that position will mean no slope overload in the following three bit "word". Since only one bit is used for polarity information, sign change of enlarged step will not

be permitted. If the polarity of the enlarged step changes within the "word", an ordinary step will be taken, i.e., no zero but either a +1 or -1 will be transmitted. The output of the MDM coder and the corresponding output of the line coder have been shown in Fig. 3.5.1 The distant decoder schematic is shown in Fig. 3.5.2

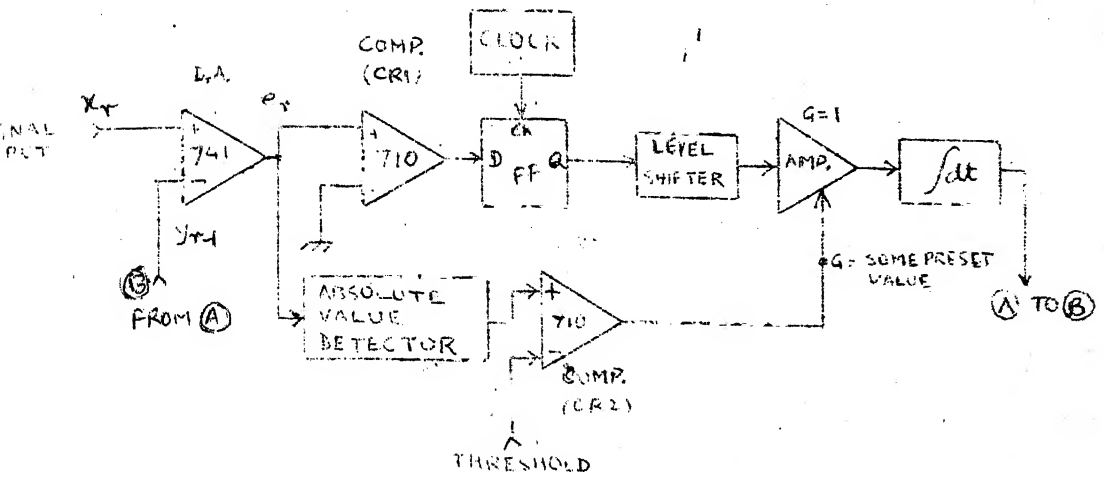


Fig-3·1: BLOCK DIAGRAM OF MDM-Type-I.

Fig-3·5·0: BLOCK DIAGRAM OF LINE ENCODING SCHEME.

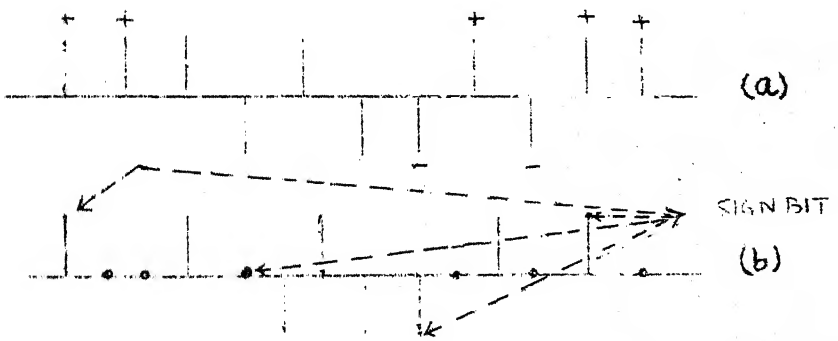


Fig-3·5·1 (a) MDM OUTPUT
(b) LINE ENCODER OUTPUT

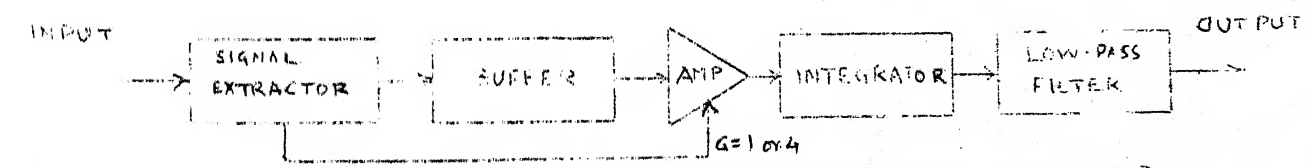


Fig-3·5·2: BLOCK DIAGRAM OF DISTANT DECODER.

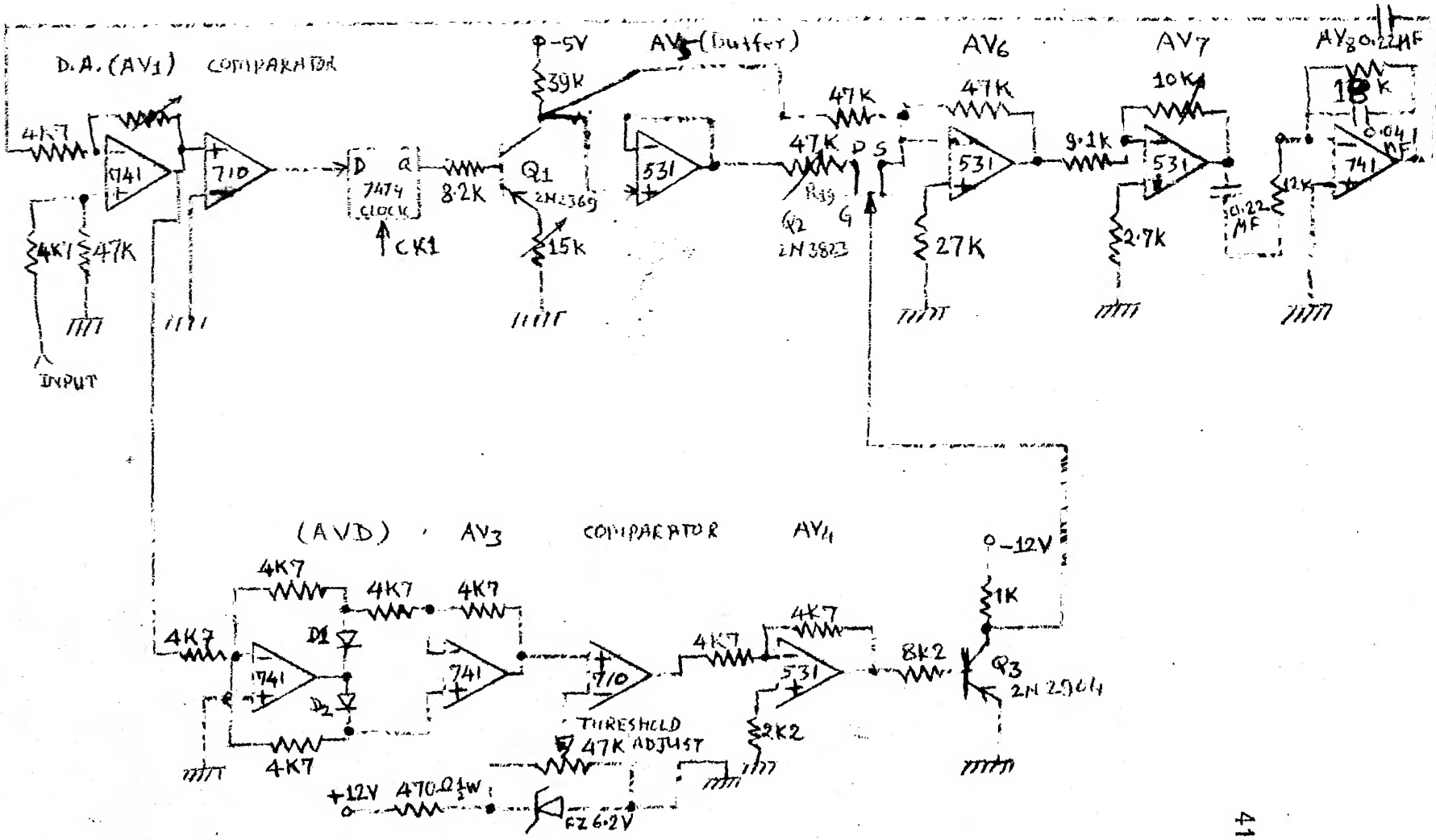


Fig. 3.2 : MODIFIED DELTA MODULATOR (MDM), TYPE – I

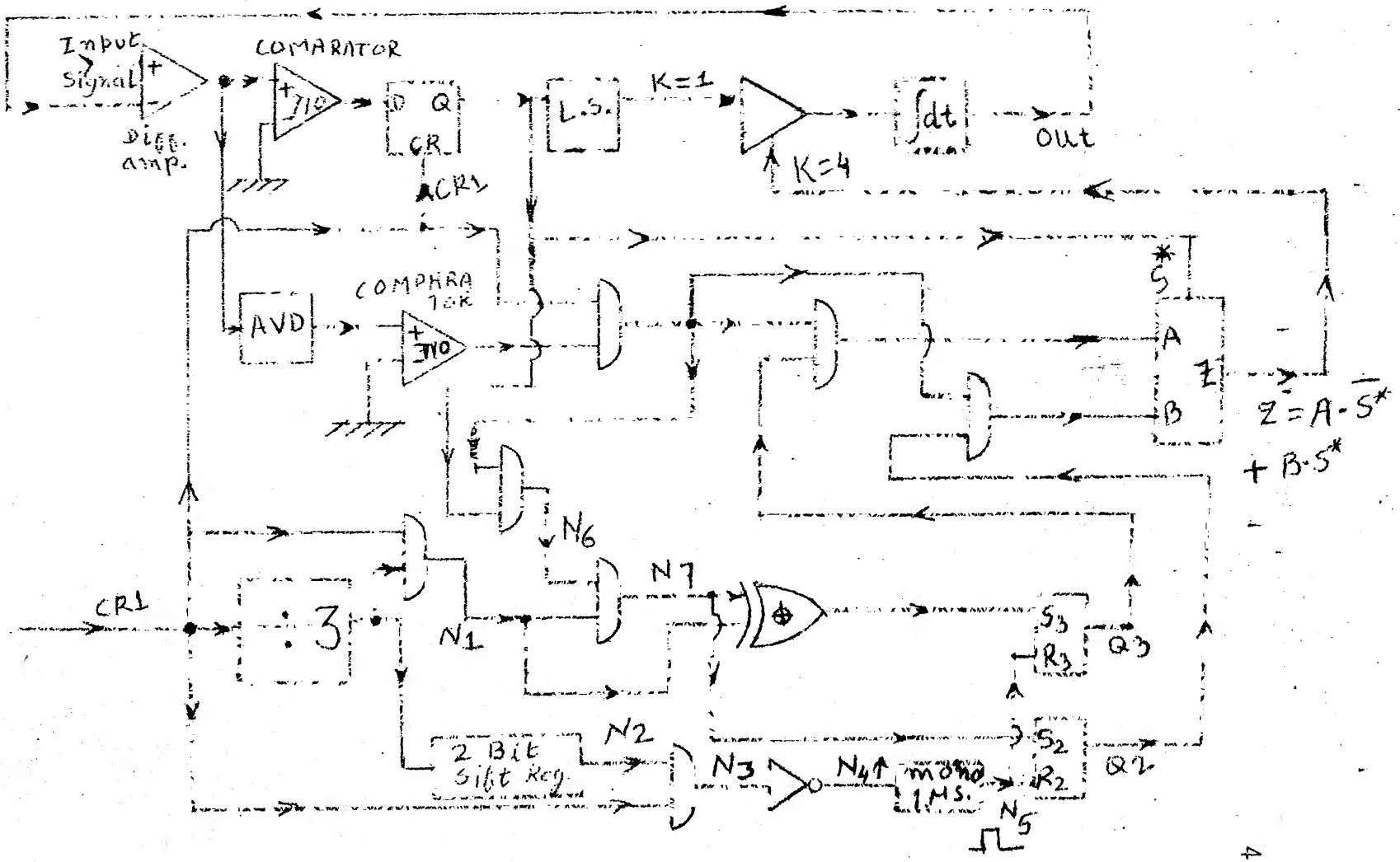


FIG. 3.3.0 BLOCK DIAGRAM OF MDM (TYPE III)

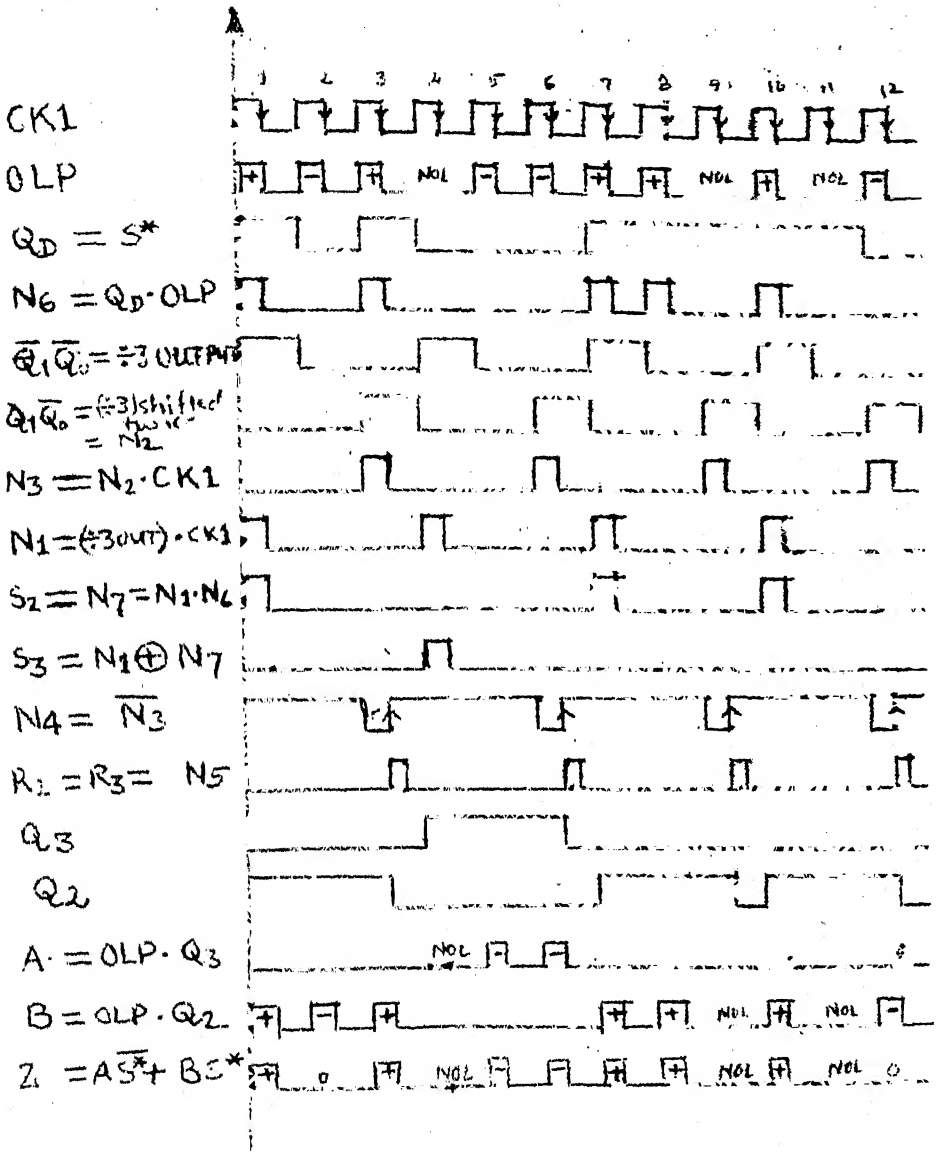


FIG 3.3.1 TIMING DIAGRAM OF MDM (TYPE III)

1	2	MDM (Type I)
1	1	MDM (Type II)
2	1	MDM (Type III)

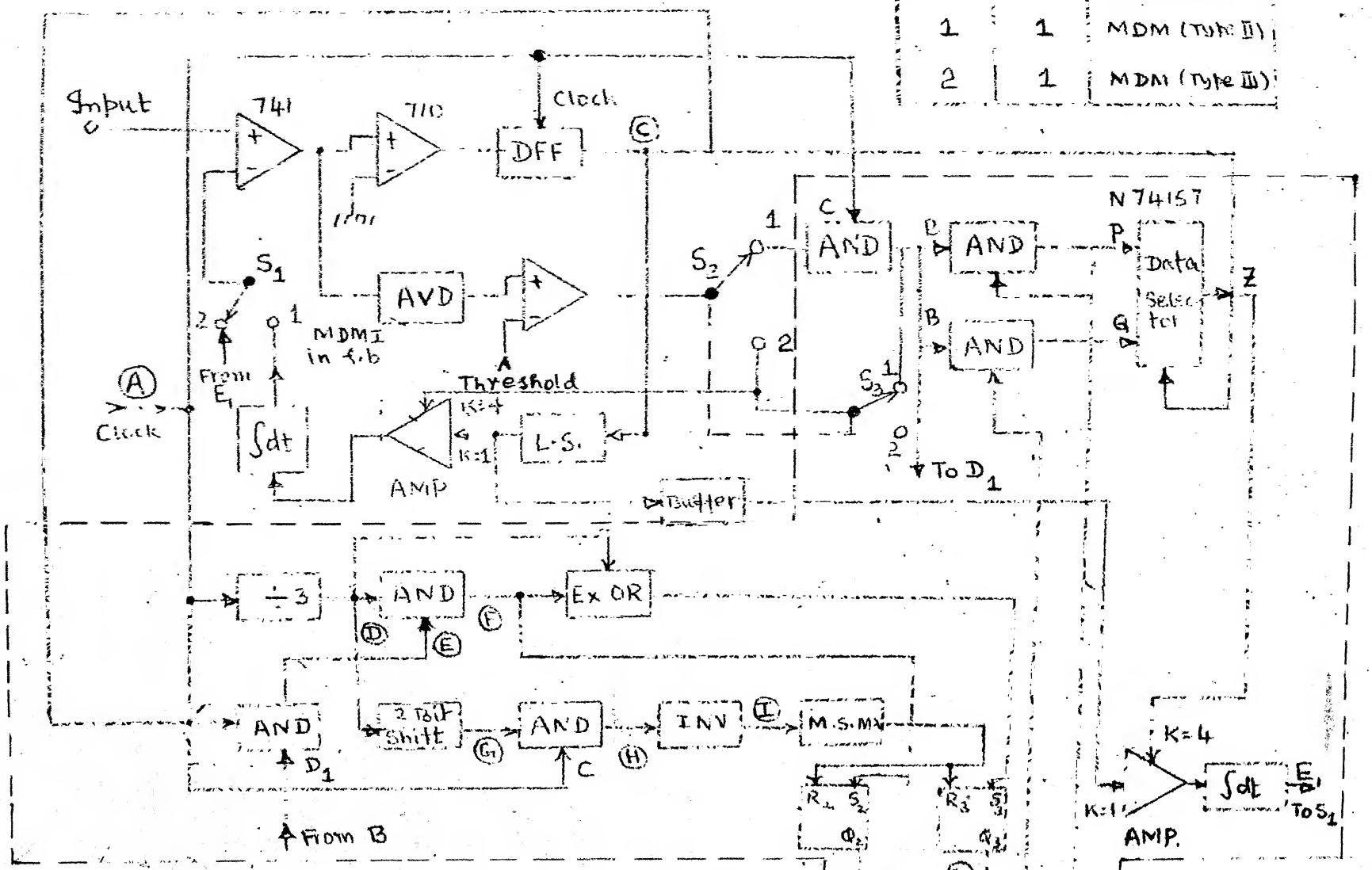


Fig 3.4 COMPLETE BLOCK DIAGRAM OF MDM TYPE I, TYPE II and TYPE III

CHAPTER 4

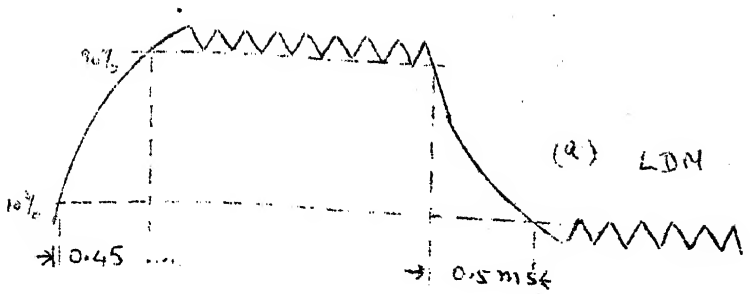
RESULTS

Responses of the linear delta modulator and the modified delta modulator (type-I) are shown in Fig. 4.1.0.

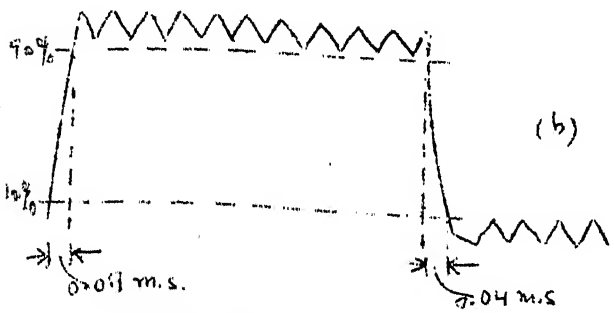
When a square wave input of pulse width (1.25 ms) is given to the systems, the linear delta modulator response is very poor as the rise time of the feed back pulse is 0.45 millisecond and the fall time is 0.5 msec. While in the modified delta modulator (Type-I), the rise time is .08 ms and the fall time is..04 ms. In the modified scheme the step size is four times the normal step size. The modified delta modulator shows inferior performance when "overload" pulses are synchronized with the clock. The rise time in this modified (type-II) case is 0.18 msec and fall time 0.1 msec. This indicates clearly that the slope "overload" pulses occur more frequently than a clock pulse. When these "overload" pulses are gated with the clock we are missing some of the "overload" pulses and thus the performance of the system is degraded.

Second modification to the delta modulator, i.e., modified system (type-III) gives better results than the modified (type-II) system. As we see from Fig. 4.1.1, the

rise time is 0.12 msec. and fall time is 0.08 msec. In this case we increase the step size by a specific factor only at the few unsuppressed "overload" pulses. This has been explained in the previous chapter. It has been observed from Fig. (4.2.0) that SNR increases when threshold level decreases. The 0.8V threshold which is twice the normal step size, gives the best result, and is in agreement with the theoretical and simulation results of Vijoy Kumar [9]. We further observe from the same plot that the over all SNR improves when the step size is kept four times the normal step size instead of three. This also verifies the theoretical and simulation results. Fig. (4.2.2) -although it does not give a very correct picture- shows that the overall SNR is inferior in this case compared to the asynchronous system having similar decrease in step size.



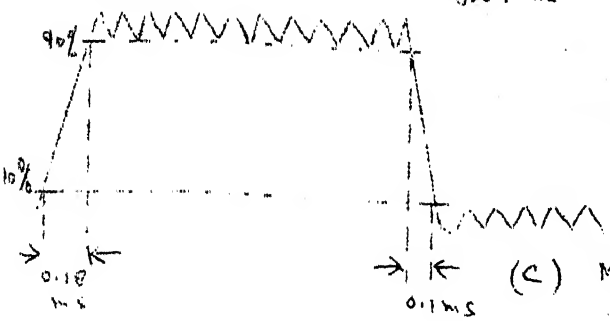
(a) LDM



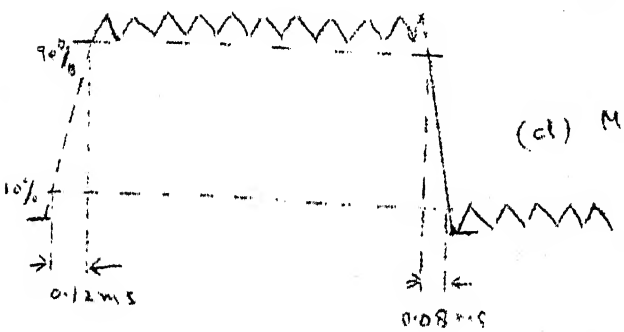
(b) MDM (Type-I)

← MDM (Type-I)

Fig: 4.1.0 Pulse RESPONSE OF ASYNCHRONUS SYSTEMS IN (a) AND (b)



(c) MDM (Type-II)



(d) MDM (Type-III)

Fig 4.1.1 PULSE RESPONSE OF SYNCHRONOUS SYSTEMS (C AND (d).

CHAPTER 5

CONCLUSION

The first system developed in the laboratory was "Adaptive Delta Modulator with One Bit Memory". The system was designed on the basis of the scheme suggested by Jayant [4], as given in Chapter 2.

The system developed in the laboratory starts giving low frequency jitter when the decoder output is fed back to the input of the comparator. Since it is difficult to analyse the closed loop system it was not possible to find out the cause for this jitter. But one of the possible reasons may be the proper selection of the adaptation constants for the system. Jayant [8]has given the values of the constants, namely A=1.1 and B = 0.909. He further mentioned that the feedback signal y(t) does not decay with time if A=1/B. It is possible that the product AB was equal to or more than unity in the experimental system, since it is not possible to adjust these small gains very accurately. Second possibility is the uncertainity of the performance of the Sample and Hold circuit in the feedback loop.

The second system developed is referred to as the modified delta modulation system. This system has been observed in two ways:

(i) when the feedback loop of the system is not synchronized with the clock, called MDM (Type-I).

(ii) when the feedback loop of the system is synchronized with the clock, called MDM (Type-II).

The peak SNR of MDM (Type-I) system is 16 dB better than LDM system when threshold voltage of the former was 0.8V, and the step size was taken four times the normal step size. Peak SNR remains unaltered but overall SNR improves by 1.5 dB when the step size is taken 3 times the normal step size. Hence, we conclude that the system which operates at threshold level of 0.8V and step size four times the normal step size, gives the best performance.

As shown in Fig.4.2, in MDM (Type-II) the overall SNR performance of the system is the same while the peak SNR of the system is slightly degraded, when the values of the threshold and the step size are taken same as in MDM (Type-I).

When the step input response of the MDM (Type-I) system is observed, we see that there is an improvement in the pulse rise and the fall time by a factor of four.

The MDM (Type-III) system, where we suppress the overload pulses of opposite polarity in a word of 3 bit sequence, gives peak SNR performance and the step input

response still better than that of MDM (Type-I) and MDM (Type-II) systems. Hardware complexity is more in MDM (Type-III) than MDM (Type-I or II), but it can be justified by the improvements.

For the ADM with one bit memory system developed in the laboratory, performance can be improved by using an analogue delay lines (order of the delay should be 20-30μs) instead of the sample and hold circuit and carefully choosing the adaptation constants.

In the known ADM systems the distant decoder should be an exact replica of the local decoder. Otherwise, some extra distortion is generated in the output. But, in the case of MDM (Type-III) the distant decoder is much simpler than the local decoder. This is an advantage for such systems.

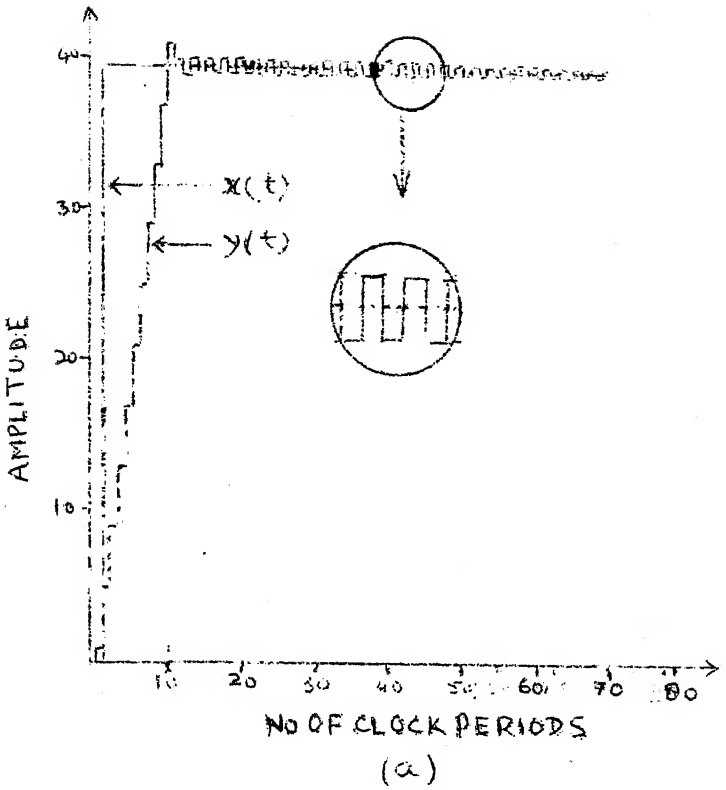
The step input response of the MDM (Types II and III) is shown in Fig. 5.1. It can be seen that the step response for this systems will in general be better than Jayant's ADM and the other ADM's described in Chapter 1.

Modified system has a draw back that as such the information regarding occurence of the overload can not be sent to the distant receiver, one possible way is to use "Line Encoding" which has been described in Chapter 3.

The line encoding plan described earlier increases the transmission rate by 1.33 times. But, this can be compensated for by the improved performance of the modified systems.

We have not seen the performance of the combined system i.e. ADM with one bit memory with MDM (Type II or III), as the ADM with one bit memory did not work satisfactorily. We can use MDM (Type II or III) system for overload input keeping the threshold at 0.8V and the step size equal to four times the normal step size and ADM with one bit memory for the under-load region of the input. The overall SNR and step input response of this combined system can be compared with the other systems already developed.

Subjective evaluation of the coder-decoder system gives the best picture in terms of its suitability in a real life situation. Therefore, it would be advisable to test the combined MDM - ADM system with speech and television signal inputs for its subjective evaluation. It is felt that the MDM system will be better suited for television signals because of its superior transient response.



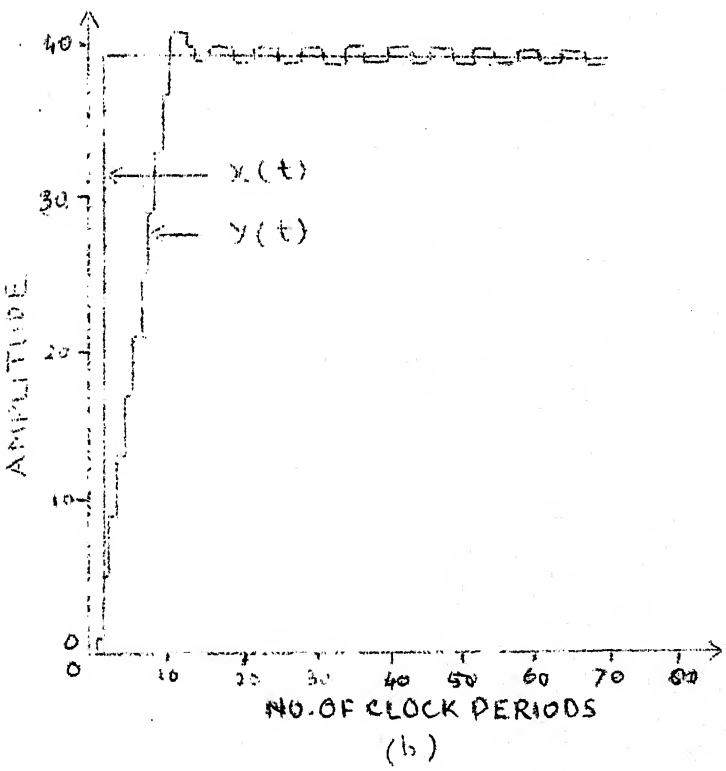


FIG: 5.1. STEP INPUT RESPONSE OF MODIFIED DM CODECS:
(a) M DM (Type-II) ; (b) M.D.M (Type-III) INITIAL STEP:

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